2.8V-6V Vin 3A Synchronous Step Down Convertor

- Qualified for Automotive Applications
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Revision 1.0: Release to production.
Revision 1.1: Update the accuracy range of V_{FB}.
Revision 1.2: Update the upper limits for I_Q, I_{SD}, V_{FB}, R_{HS}, and R_{LS}.
Revision 1.3: Update T_J in RECOMMENDED OPERATING CONDITIONS.
Revision 1.4: Update DEVICE ORDER INFORMATION and the parameter of $ILIM_{LS}$.

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2130QFTAR	Tape & Reel	3000	130Q	8	FCQFN2x1.5-8

ELECTRICAL CHARACTERISTICS

IN -40 ~125 , typical values

j=25° C 0 0

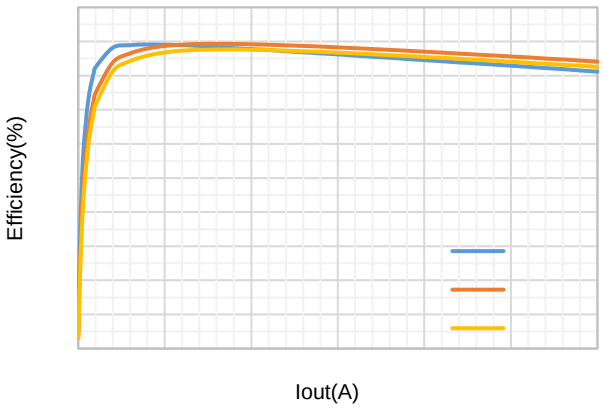


Figure 1. Efficiency vs Load Current, Vout=1.2V

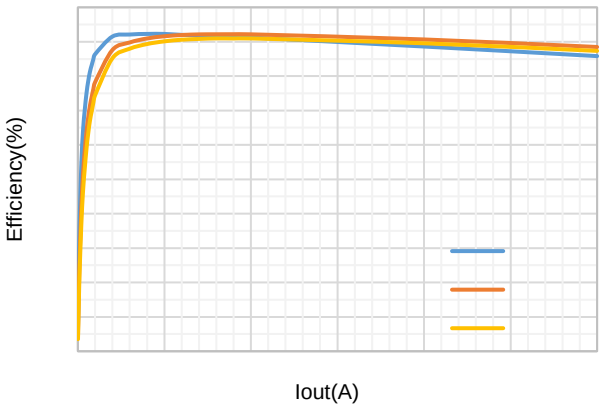
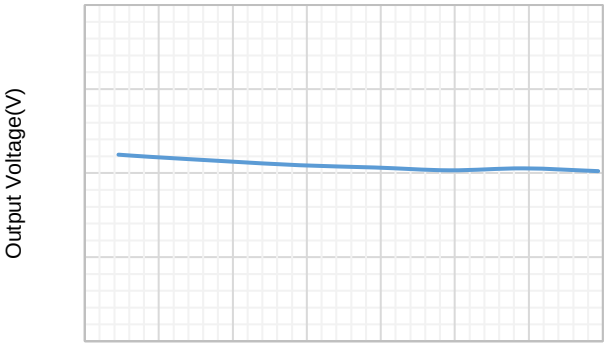


Figure 2. Efficiency vs Load Current, Vout=1.8V



317.051 0 0 1 125l98.174 5[1)-9(.)11(:

Figure 3. Line Regulation, Io=1.5A

Figure 4. Load Regulation, Vin=5V

Figure 5. V_{FB} vs Temperature

Figure 6. UVLO vs Temperature

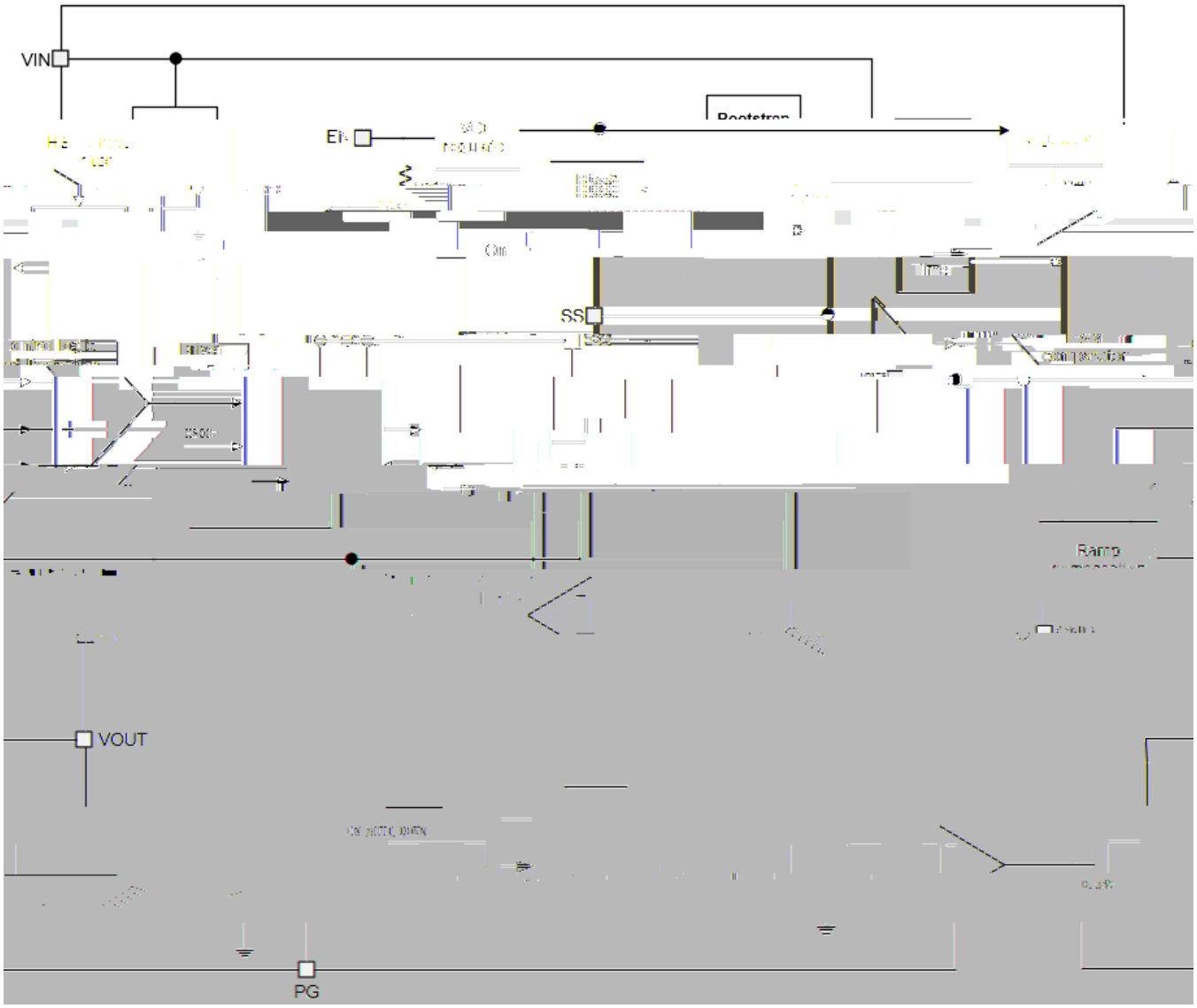


Figure 7. Functional Block Diagram

Overview

The SCT2130Q is a 2.8V-6V input, 3A output, synchronous buck converter with built-in 25m high-side and 20m Rdson low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response, and internal error amplifier integrated improve the line and load regulation.

The switching frequency is fixed 2.1MHz. The SCT2130Q features programmable soft start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The SCT2130Q operates in Forced Continuous Conduction Mode (FCCM) to achieve low light load ripple. The quiescent current is typically 1000uA under no load and no switching.

The SCT2130Q full protection features include the input under-voltage lockout, over current protection with cycle-by-

SCT2130Q

voltage is pulled to GND to indicate an output failure. If VIN and EN are not available, and PG is pulled up by an external power supply, PG will self- -up resistor is used, the voltage on the pin is below 0.4V.

Thermal Shutdown

Once the junction temperature in the SCT2130Q exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2K . Use Equation 4 to calculate R1.

(7)

(8)

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2130Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 12 desired.

(12)

Where:

- is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10

Application Waveforms

V_{IN}=5V, V_{OUT}=1.2V, unless otherwise noted

Figure 9. Power up (I_{LOAD}=3A)

Figure 10. Power down (

Application Waveforms

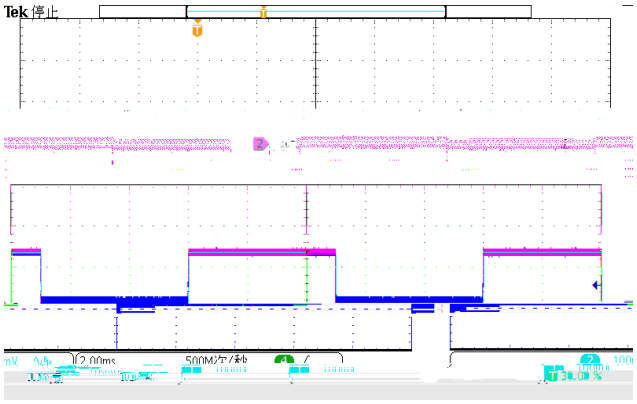


Figure 15. Load Transient (0.3A-2.7A, 1.6A/us)

Figure 16. Load Transient (0.75A-2.25A, 1.6A/us)

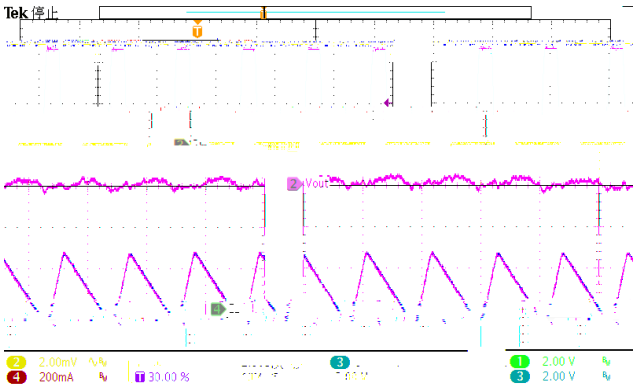


Figure 17. Output Ripple (I_{LOAD}=100mA)

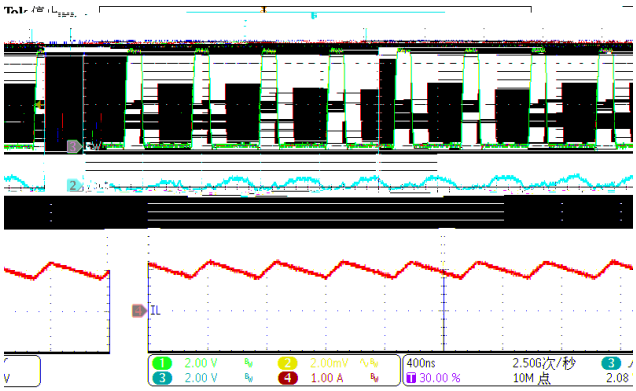


Figure 18. Output Ripple (I_{LOAD}=1A)

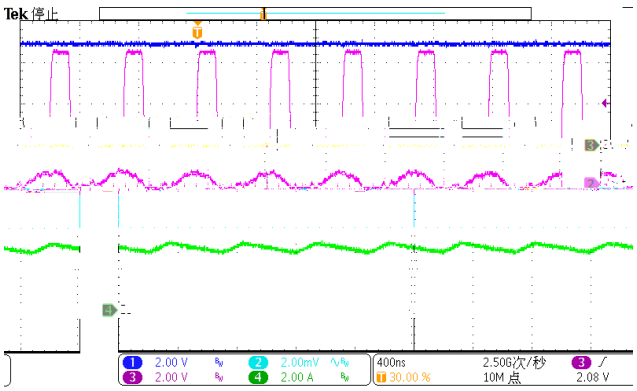


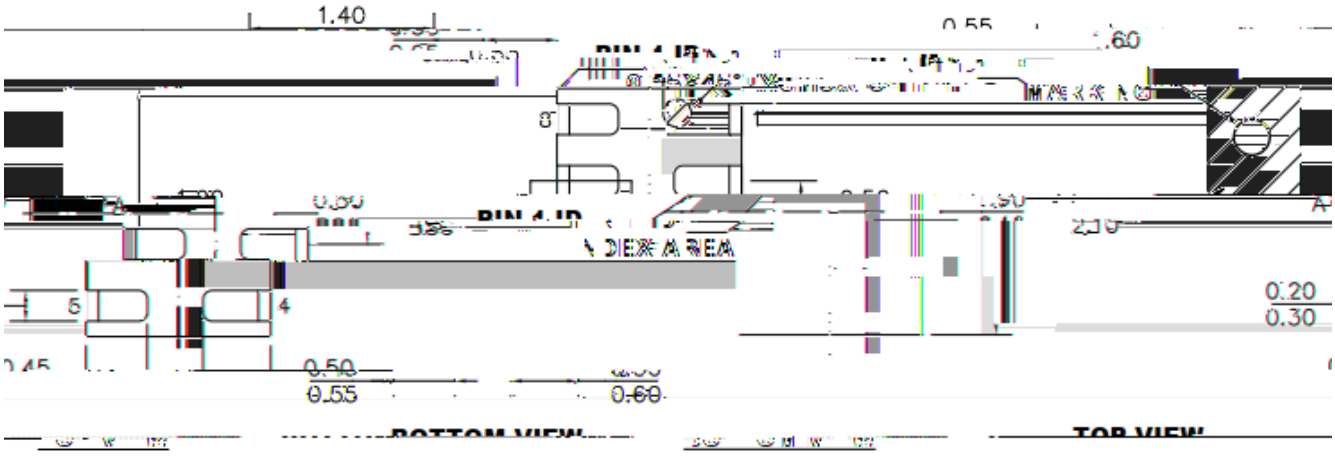
Figure 19. Output Ripple (I_{LOAD}=3A)

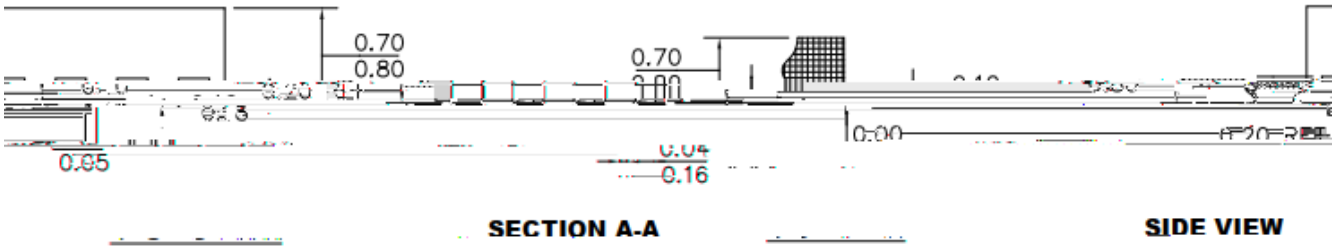
Figure 20. Thermal, V_{IN}=5V, V_{OUT}=1.2V, I_{LOAD}=3A

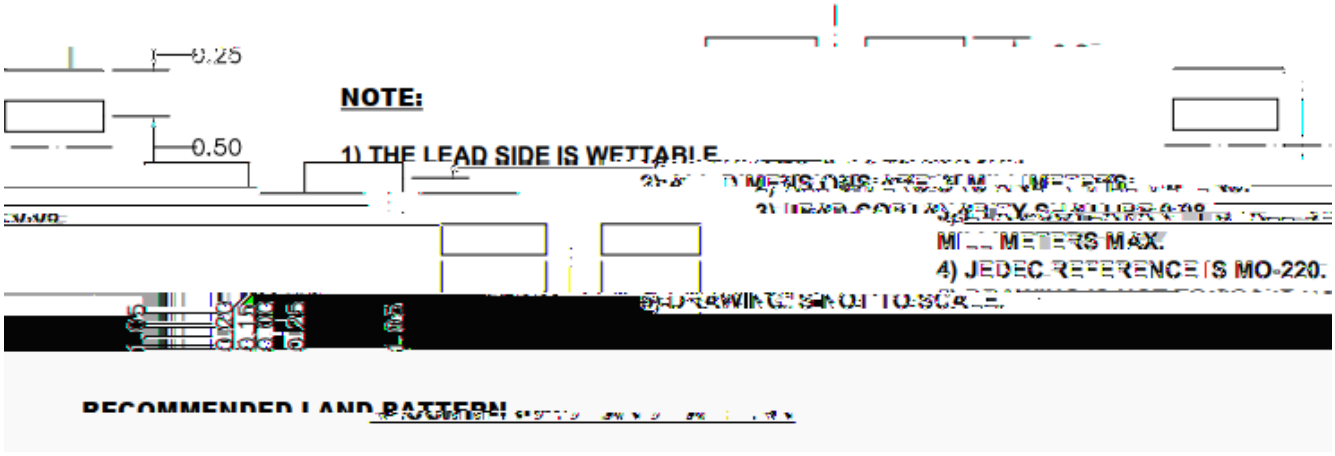
Layout Guideline

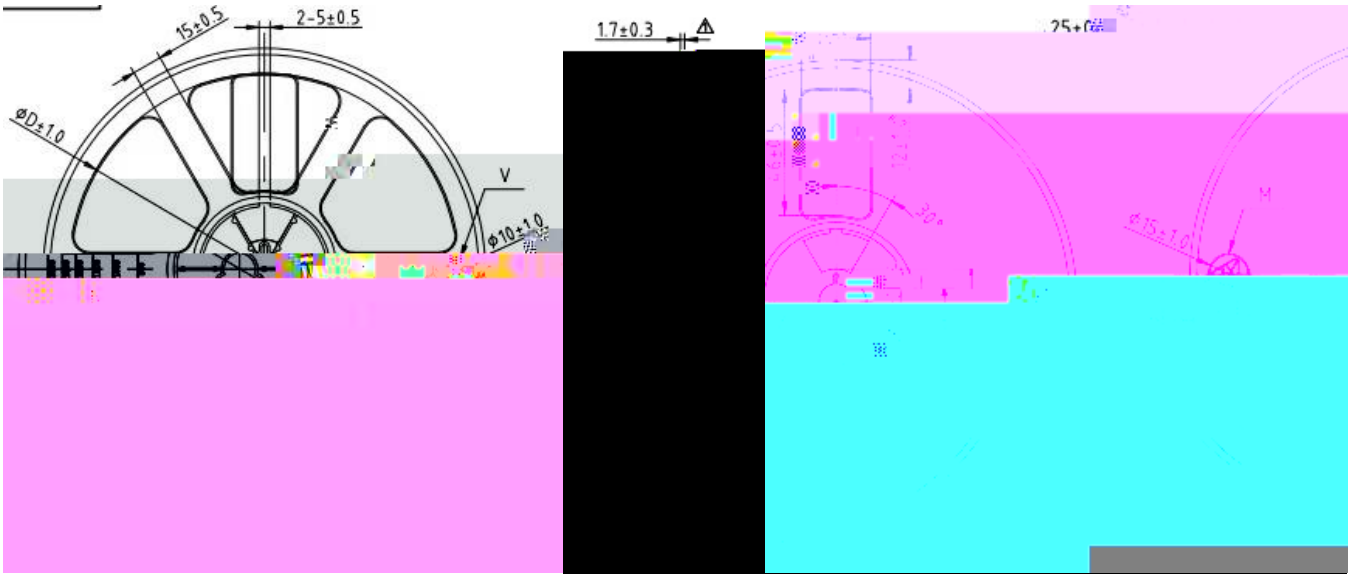
Proper PCB layout is a critical for SCT2130Q operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

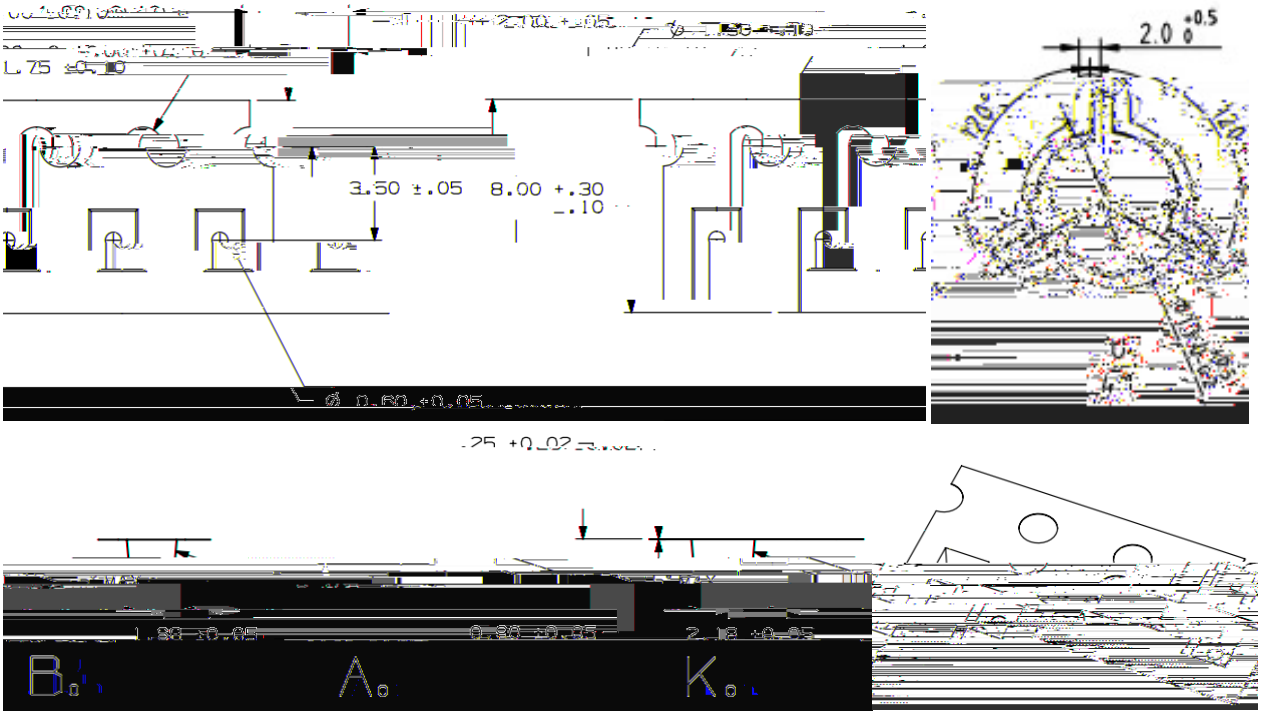
1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2.











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